

Please delete the paragraph heading on page 16 of the subject application, line 1, and insert in place thereof the paragraph heading as follows:

--CLAIMS--

Please insert the paragraph heading on page 16 of the subject application, before claim 1, the following:

-- What is claimed is: --.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) Method for fabricating a semiconductor structure having a plurality of gate stacks (~~GS1, GS2, GS3, GS4~~) on a semiconductor substrate (~~10~~), having the following steps:
 - (a) application of the gate stacks (~~GS1, GS2, GS3, GS4~~) to a gate dielectric (~~11~~) above the semiconductor substrate (~~10~~);
 - (b) formation of a sidewall oxide (~~17~~) on sidewalls of the gate stacks (~~GS1, GS2, GS3, GS4~~);
 - (c) application and patterning of a mask (~~12~~) on the semiconductor structure; and
 - (d) implantation of a contact doping (~~13~~) in a self-aligned manner with respect to the sidewall oxide (~~17~~) of the gate stacks (~~GS1, GS2~~) in regions not covered by the mask (~~12~~).
2. (Currently Amended) Method according to claim 1, ~~characterized in that~~ wherein, after the implantation of the contact doping (~~13~~), the sidewall oxide (~~17~~) is reduced in its lateral extent in regions not covered by the mask (~~12~~).
3. (Currently Amended) Method according to claim 2, ~~characterized in that~~ wherein the reduction of the extent of the lateral sidewall oxide (~~17'~~) is followed by a further implantation of different doping (~~18~~).
4. (Currently Amended) Method according to claim 3, ~~characterized in that~~ wherein the further doping (~~18~~) is a p-type doping having a low concentration, preferably with a dopant concentration that is at least a power of ten lower than the contact doping concentration.
5. (Currently Amended) Method according to claim 3, ~~characterized in that~~ wherein the further doping (~~18~~) is a bit line halo doping implanted from a predetermined direction at a predetermined angle (~~α~~), preferably in the range of between 0° and 30° inclusive.
6. (Currently Amended) Method according to ~~one of the preceding claims,~~ claim 1, wherein the contact doping (~~13~~) is implanted at a predetermined angle (~~α~~) of $\alpha = 0^\circ$.
7. (Currently Amended) Method according to ~~one of the preceding claims,~~ claim 1, wherein the contact doping (~~13~~) is an n-type doping having a high concentration, for example having an implantation dose of about 10^{14} to $3 \cdot 10^{15}/\text{cm}^2$, preferably with arsenic.

8. (Currently Amended) Method according to ~~one of the preceding claims,~~ characterized in that claim 1, wherein a removal of the mask (12) is followed by an implantation of a, preferably identical, dopant having a lower dopant concentration than that of the contact doping (13).
9. (Currently Amended) Method according to ~~one of the preceding claims,~~ characterized in that claim 1, wherein the gate stacks (~~GS1, GS2, GS3, GS4~~) are applied approximately equidistantly with respect to one another, a storage capacitor (TK) being arranged alternately below every third or first adjacent gate stack (~~GS3, GS4~~) in the semiconductor substrate (10) in a cross-sectional plane.
10. (Currently Amended) Method according to ~~one of the preceding claims,~~ characterized in that claim 1, wherein the method is used for fabricating logic transistors.
11. (Currently Amended) Method according to ~~one of the preceding claims,~~ characterized in that claim 1, wherein the method is used for fabricating selection transistors, preferably of a DRAM.
12. (Currently Amended) Method according to ~~one of the preceding claims,~~ characterized in that claim 1, wherein the gate stacks (~~GS1, GS2~~) are fabricated with a length of less than 200 nm.
13. (Currently Amended) Method according to ~~one of the preceding claims,~~ characterized in that claim 1, wherein the gate stacks (~~GS1, GS2~~) are provided parallel and in strip-type fashion on the semiconductor substrate (10).
14. (Currently Amended) Method according to ~~one of the preceding claims,~~ characterized in that claim 1, wherein the gate stacks (~~GS1, GS2~~) have a lower first layer (14) made of polysilicon and an overlying second layer (15) made of a metal silicide or a metal.
15. (Currently Amended) Method according to ~~one of the preceding claims,~~ characterized in that claim 1, wherein the gate stacks (~~GS1, GS2~~) are created by carrying out an application and patterning of the first layer (14), the overlying second layer (15) and a third layer (16) arranged thereon on the gate dielectric (11).
16. (Currently Amended) Method according to claim 15, ~~characterized in that~~ wherein the third layer (16) has silicon nitride or oxide.